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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/684,611	10/06/2000	Guy Meynants	M-11283 US	3244

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Jack V Musgrove
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EXAMINER

LONG, HEATHER R

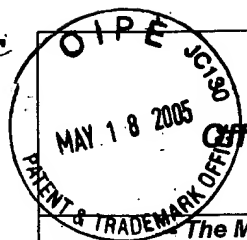
ART UNIT PAPER NUMBER

2615

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary

Application No.	Applicant(s)	
09/684,611	MEYNANTS, GUY	
Examiner	Art Unit	
Heather R. Long	2615	

The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 December 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 October 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 4/1/2002.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. Applicant's election with traverse of the amplifying circuit in the reply filed on 12/6/2004 is acknowledged. The traversal is on the ground(s) that all the species illustrate an amplifying circuit for a pixel array in an imaging device and that the same reference numbers are used through the different embodiments. This is not found persuasive because each embodiment has different characteristics that are unique to that particular embodiment, which create a burdensome search on the examiner. Furthermore, the Applicant has failed to prove that these characteristics would not create be a burdensome search. Therefore, the requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Dierickx et al. (WO 99/16238).

Regarding claim 1, Dierickx et al. discloses in Fig. 2 an amplifying circuit, comprising: an amplifying element (A1) with at least an input terminal and an output terminal, a signal input node (11), the signal levels of which at least two moments in time are to be amplified by the amplifying element (page 11, lines 6-

9), at least two connecting lines between the signal input node and the amplifying element (these lines can be seen in Fig. 2), for transferring a signal from the signal input node to the input terminal of the amplifying element, a memory element (MR1 or MS1) on at least one of the connecting lines, for storing a signal level of the signal input node at a moment in time (page 11, lines 15-27), a switching element disposed on each connecting line (S41 and S51), between the memory element and the input terminal of the amplifying element if a memory element is provided on the connecting line, for consecutively connecting signal levels of the signal input node at different moments in time to the same amplifying element, at least one output node (can be seen in Fig. 2), each output node being connected to the output terminal of the same amplifying element.

Regarding claim 2, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 1 as well as disclosing that the amplifying circuit comprises a memory element on each of the connecting lines (MR1 and MS1).

Regarding claim 3, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 1 including that there are the same number of output nodes as there are connecting lines (as can be seen in Fig. 2, there is one output line and one connecting line), output nodes and connecting lines being associated with each other according to a 1 to 1 relationship, each output node being consecutively connected over the same amplifying element to the connecting line with which it is associated (this can be seen in Fig 2).

Regarding claims **4** and **5**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 1 including that the amplifying element is a transistor or a transistor of the type of metal oxide semiconductor transistors. (It is inherent that the amplifying element is a transistor or a transistor of the type of metal oxide semiconductor transistors).

Regarding claim **6**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 1 including that the amplifying element is an operational transconductance amplifier (It is inherent that the amplifying element is an operational transconductance amplifier).

Regarding claim **7**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 1 including that the memory element is a capacitor (page 11, lines 20-21 and 27).

Regarding claim **8**, Dierickx et al. discloses in Fig. 2 an array of amplifying circuits, each amplifying circuit, comprising: an amplifying element (A1) with at least an input terminal and an output terminal, a signal input node (I1), the signal levels of which at least two moments in time are to be amplified by the amplifying element (page 11, lines 6-9), at least two connecting lines between the signal input node and the amplifying element (these lines can be seen from Fig. 2), for transferring a signal from the signal input node to the input terminal of the amplifying element, a memory element (MR1 or MS1) on at least one of the connecting lines, for storing a signal level of the signal input node at a moment in time (page 11, lines 15-27), a switching element disposed on each connecting

line (S41 and S51), between the memory element and the input terminal of the amplifying element if a memory element is provided on the connecting line, for consecutively connecting signal levels of the signal input node at different moments in time to the same amplifying element, at least one output node (can be seen in Fig. 2), each output node being connected to the output terminal of the same amplifying element, the array further comprising: at least one output line (Y) in common to all amplifying circuits of the array, the output nodes of the amplifying circuits being connected to the output lines.

Regarding claim 9, Dierickx discloses in Fig. 2 a device for imaging applications, comprising: a matrix of active pixels arranged in a geometric configuration, each pixel producing an electrical signal indicative of the light intensity of a portion of a scene being imaged by that pixel (page 1, lines 25-32), at least one amplifying circuit common to a group of pixels out of the matrix, at least one output line wherein each amplifying circuit comprises an amplifying element (A1) with at least an input terminal and an output terminal, a signal input node (I1) being intended to obtain electrical signals from pixels out of the group of pixels to which the amplifying circuit is common, the signal levels of are to be amplified by the amplifying element (page 11, lines 6-9), at least two connecting lines between the signal input node and the amplifying element (these lines can be seen in Fig. 2), for transferring an electrical signal from the signal input node to the input terminal of the amplifying element, a memory element (MR1 or MS1) on at least one of the connecting lines, for storing a signal level of the electrical

signals at the signal input node at a moment in time (Page 11, lines 15-27), a switching element disposed on each connecting line, between the memory element and the input terminal of the amplifying element if a memory element is provided on the connecting line (S41 and S51), for consecutively connecting signal levels of the signal input node at different moments in time to the same amplifying element, at least one output node (can be seen in Fig. 2), each output node being connected to the output terminal of the same amplifying element.

Regarding claim **10**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 9 including that the matrix is arranged in columns and rows and wherein the group of pixels is a row of pixels (Fig. 2).

Regarding claim **11**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 9 including that the matrix is arranged in columns and rows and wherein the group of pixels is a column of pixels (Fig. 2).

Regarding claim **12**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 9 including that the output lines (11) are common to the matrix of active pixels, the output node of each amplifying circuit being connected to the output lines (Y).

Regarding claim **13**, Dierickx et al. discloses all the limitations as previously discussed with respect to any of the claims 9-12 as well as disclosing that the device may be used in camera systems or imaging applications requiring a high image quality (page 1, lines 15-19).

Regarding claim **14**, Dierickx et al. discloses a pixel adapted for integration in an imaging device, comprising: a radiation sensitive element able to produce an electrical signal indicative of the amount of radiation picked up by that pixel (page 1, lines 25-32), an amplifying circuit wherein the amplifying circuit comprises an amplifying element (A1) with at least an input terminal and an output terminal, a signal input node (I1), the signal levels of which at least two moments in time are to be amplified by the amplifying element the signal levels being obtained from the radiation sensitive element (page 11, lines 6-9), at least two connecting lines between the signal input node and the amplifying element (these lines can be seen in Fig. 2), for transferring a signal from the signal input node to the input terminal of the amplifying element, a memory element (MR1 or MS2) on at least one of the connecting lines, for storing a signal level of the signal input node at a moment in time (page 11, lines 15-27), a switching element disposed on each connecting line (S41 and S51), between the memory element and the input terminal of the amplifying element if a memory element is provided on the connecting line, for consecutively connecting signal levels of the signal input node at different moments in time to the same amplifying element, at least one output node (can be seen in Fig. 2), each output node being connected to the output terminal of the same amplifying element.

Regarding claim **15**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 14 including that the radiation sensitive element is a photodiode (page 1, lines 25-32).

Regarding claim **16**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 14 including that the radiation sensitive element is an infrared photodetector (page 1, lines 25-32).

Regarding claim **17**, Dierickx et al. discloses a method for reducing fixed pattern noise of solid state imaging device having a group of active pixels (page 4, lines 30-35), each pixel comprising a radiation sensitive element (page 1, lines 25-32) and an amplifying circuit, the method comprising the following steps: reading out the signal of a pixel brought in a first state and storing the corresponding voltage level in a first memory element, reading out the signal of the pixel brought in a second state (which is different from the first state) and storing the corresponding voltage level in a second memory element (page 11, lines 15-28), transferring the signal of the first memory element to an amplifying element, amplifying it and transferring it to an output line, transferring the signal of the second memory element to the same amplifying element, amplifying it and transferring it to an output line, repeating these steps for at least part of the pixels of the imaging device (page 11, line 29 – page 12, line 8).

Regarding claim **18**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 17 including that the memory element uses one output line (can be seen in Fig. 2).

Regarding claim **19**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 17 as well as disclosing that it further

comprises the step of calculating a differential output signal by taking the difference between potential values on the output lines (page 3, lines 10-23).

Regarding claim **20**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 17 including that the first state and the second state correspond to different amounts of radiation collected on the radiation sensitive element in the pixel (page 11, lines 15-28).

Regarding claim **21**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 20 including that the first state or second state corresponds to an amount of radiation or light collected on the radiation sensitive element in the pixel (page 11, lines 15-28).

Regarding claim **22**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 20 including that the second state or the first state corresponds to a non-irradiated or non-illuminated or dark or reset state of the pixel (page 11, lines 15-28).

Regarding claim **23**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 17 including that the pixel is read out in additional states and its corresponding voltage level is being stored on additional memory elements (page 1, line 25 – page 4 lines 7; page 11, lines 6 – page 12, line 20).

Regarding claim **24**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 17 including that the signal of the first memory element is transferred to the first output line common for the group, and

concurrently, the signal of the second memory element of another amplifier is transferred to the second output line common for the group (Fig. 3).

Regarding claim **25**, Dierickx discloses a method for reducing fixed pattern noise and kTC noise in a solid state imaging device having a group of active pixels (page 10, lines 29-35), each pixel comprising a radiation sensitive element (page 1, lines 25-32) and an amplifying circuit, the method comprising the following steps: reading out the signal of a pixel brought in a first state, corresponding to the non-illuminated or dark condition of the pixel or to the reset state of the pixel, and storing the corresponding voltage level alternately on a first or a third memory element, reading out the signal of the pixel in a second state, at a later moment in time, corresponding to an amount of radiation or light collected on the radiation sensitive element on the pixel, and storing the corresponding voltage level on a second memory element alternately (page 11, lines 15-27), transferring the signal of the first or third memory element to an amplifying element, amplifying it and transferring it to an output line that is common to the group of pixels, transferring the signal of the second memory element to the same amplifying element, amplifying it and transferring it to an output line that is common to the group of pixels, repeating this operation for essentially all or part of the pixels of the imaging device (page 11, line 29 – page 12, line 8).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather R. Long whose telephone number is 571-272-7368. The examiner can normally be reached on Mon. - Thurs.: 7:00 am - 4:30 pm, and every other Fri.: 7:00 am - 3:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, James Groody can be reached on 571-272-7950. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Heather R Long
Examiner
Art Unit 2615

HRL
May 2, 2005


TUAN HO
PRIMARY EXAMINER

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Notice of References Cited

Application/Control No.

09/684,611

Applicant(s)/Patent Under
Reexamination
MEYNANTS, GUY

Examiner

Heather R. Long

Art Unit

2615

Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	WO 99/16238	04-1999		Dierickx, et al.	H04N 5/217
	O					
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NON-PATENT DOCUMENTS

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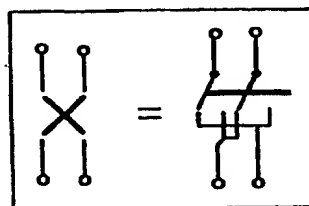
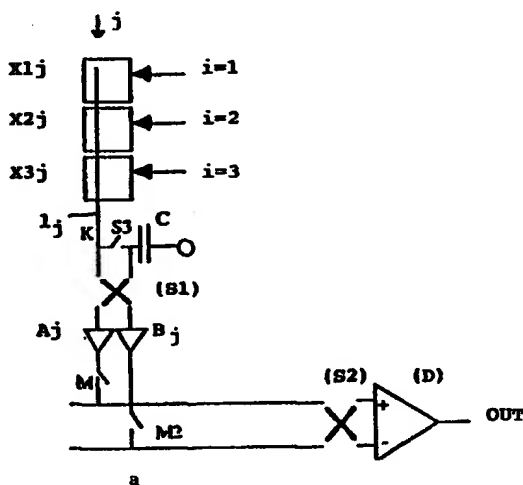
INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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			(43) International Publication Date: 1 April 1999 (01.04.99)
(21) International Application Number: PCT/BE98/00139 (22) International Filing Date: 22 September 1998 (22.09.98) (30) Priority Data: 97870143.1 22 September 1997 (22.09.97) EP 97870170.4 24 October 1997 (24.10.97) EP (71) Applicant (for all designated States except US): INTERUNIVERSITAIR MICRO-ELEKTRONICA CENTRUM [BE/BE]; Vereniging Zonder Winstbejag, Kapeldreef 75, B-3001 Heverlee (BE). (72) Inventors; and (75) Inventors/Applicants (for US only): DIERICKX, Bart [BE/BE]; Cornelis Deherdstraat 8, B-2640 Molsel (BE). KAVADIAS, Spyros [GR/BE]; Predikherinnenstraat 6, B-3000 Leuven (BE). (74) Agents: VAN MALDEREN, Joëlle et al.; Office Van Malderen, Place Reine Fabiola 6/1, B-1083 Brussels (BE).		(81) Designated States: AL, AU, BA, BB, BG, BR, CA, CN, CU, CZ, DE, DE (Utility model), EE, GD, GE, HR, HU, ID, IL, IS, JP, KP, KR, LC, LK, LR, LT, LV, MG, MK, MN, MX, NO, NZ, PL, RO, SG, SI, SK, SL, TR, TT, UA, US, UZ, VN, YU, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG). Published With international search report.	

(54) Title: DEVICES AND METHODS FOR IMPROVING THE IMAGE QUALITY IN AN IMAGE SENSOR

(57) Abstract

The present invention is related to an image sensor comprising an array of rows (i) and columns (j) of pixels (X_{ij}), all the pixels of one column of the array being connected to at least one common pixel output line (l_j) having at least one memory element (M_j) and at least a first amplifying element (A_j), all these amplifying elements (A_j) being connected to a common output amplifier (D). According to one preferred embodiment, said image sensor comprises: a second amplifying element (B_j) on the output of the memory element (M_j); said common output amplifier (D) having at least two input terminals; means (S1) for switching the pixel's signal on the common output line (l_j) and the memory element's signal (M_j) to respectively third and second amplifying element (A_j and B_j) of one column; and means (S2) for switching the two output signals of the amplifying elements (A_j , B_j) of one column to respectively first and second input terminals of said common output amplifier (D).



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5

DEVICES AND METHODS FOR IMPROVING THE IMAGE QUALITY IN AN
IMAGE SENSOR

10

Field of the invention

The present invention relates to solid state imaging devices being manufactured in a CMOS- or MOS-technology.

15

More particularly, the principal object of the present invention is related to methods and devices which are able to improve the image quality in an image sensor.

Another object of the present invention is related to the improvement of the image quality by a method of correcting isolated pixel values present in an image taken by imaging devices.

Background of the invention

25 Solid state image sensors are well known. Virtually all solid-state imaging sensors have as key element a photosensitive element being a photoreceptor, a photo diode, a photo transistor, a CCD gate, or alike. Typically, the signal of such a photosensitive element is a
30 current which is proportional to the amount of electromagnetic radiation (light) falling onto the photosensitive element.

A structure with a photosensitive element included in a circuit having accompanying electronics is

called a pixel. Such pixel can be arranged in an array of pixels so as to build focal plane arrays of rows and columns.

Commonly such solid state image sensors are
5 implemented in a CCD-technology or in a CMOS- or MOS-technology. Solid state image sensors find a widespread use in devices such as camera systems. In this application a matrix of pixels comprising light sensitive elements constitutes an image sensor, which is mounted in the camera
10 system. The signal of said matrix is measured and multiplexed to a so-called video-signal.

Of the image sensors implemented in a CMOS- or MOS-technology, CMOS or MOS image sensors with passive pixels and CMOS or MOS image sensors with active pixels are
15 distinguished. An active pixel is configured with means integrated in the pixel to amplify the charge that is collected on the light sensitive element. Passive pixels do not have said means and require a charge sensitive amplifier that is not integrated in the pixel. For this
20 reason, active pixel image sensors are potentially less sensitive to noise fluctuations than passive pixels. Due to the additional electronics in the active pixel, an active pixel image sensor may be equipped to execute more sophisticated functions, which can be advantageous for the
25 performance of the camera system. Said functions can include filtering, operation at higher speed or operation in more extreme illuminations conditions.

Examples of such imaging sensors are disclosed in EP-A-0739039, in EP-A-0632930 and in
30 US-A-5608204. The imaging devices based on the pixel structures as disclosed in these patent applications however are still subject to deficiencies in the image quality of the devices.

A problem in these CMOS based imaging devices appears because material imperfections and technology variations have as effect that there is a non-uniformity in the response of the pixels in the array. This effect is
5 caused by a non-uniformity or fixed pattern noise (FPN) or by a photoresponse non-uniformity (PRNU). Correction of the non-uniformity needs some type of calibration, e.g. by multiplying or adding/subtracting the pixel's signals with a correction amount that is pixel-dependent.

10 Several methods to cancel FPN are based on techniques that are often called correlated double sampling or offset compensation. The methods in general are based on the following: the signal of the pixel is subtracted from the signal of the same pixels in a reference state (this
15 reference state is typically the reset or dark state). The difference of both signal is free of pixel-related non-uniformity. However, if the differencing circuit is common for a part of the imager (typically, common for one column), a new non-uniformity will originate due to the
20 non-uniformity of the differencing circuits. In a typical APS imager with common column buffers or column amplifiers, the new fixed pattern noise is column dependent, and is visible in the image as a shade of vertical stripes.

A stripe-shaped FPN is much more annoying
25 than a pure statistical FPN. It is seen in experiments that a true random FPN of 5% RMS is barely visible to the human eye, whereas a stripe-shaped FPN remains visible even when the amplitude is below 1% RMS. The reason is that the human eye has a kind of built-in spatial filter that recognises
30 larger structures even when they have low contrast.

Even if in the case that we have no fixed pattern noise, the photoresponse non-uniformity can be different from 0.

Another problem arises due to processing imperfections, statistics, etc. This means that typically, a finite number of pixels in a pixel array will be defective (hard faults) or yield a signal that deviates
5 visibly from the "exact" pixel value. Such faults appear as white or black (or grey) points in the image. This class of faults in the sequel is called an isolated pixel value.

A known way to cancel these spots is to store a list of them and of their positions in the image in a
10 memory unit in the device. In an image processing step, the isolated pixel value is then replaced by e.g. the average of the surrounding pixels. This method is viable, but has the disadvantage that it requires a memory. Moreover, it cannot handle isolated pixel values that appear
15 intermittently or only in certain cases. A good example, is a so-called dark current pixel. Such pixels will appear white in a dark environment, but will behave normal in a bright environment.

Other ways to cancel isolated pixels faults
20 have been proposed, e.g. the spatial median filter or other types of Kalman filters can be used to remove such isolated faults. Unfortunately, such filters do also remove useful detail from the image. Consider the image of a star covered sky with an image sensor that has some faulty pixels that
25 appear white. The quoted filters are not able to remove the white point due to faults, and leave the white points that are stars untouched.

Aim of the invention

30 The present invention aims to suggest a pixel structure and methods to improve the image quality, more in particular the image non-uniformity of in array of pixels by cancellation of the appearance of column-shaped fixed pattern noise (FPN).

Main characteristics of the present invention

As a first object, the present invention is related to an image sensor comprising an array of rows and columns of pixels, all the pixels of one column of the array being connected to at least one common pixel output line having at least one memory element and at least a first amplifying element, all these amplifying elements being connected to a common output amplifier.

According to one preferred embodiment, the image sensor further comprises :

- a second amplifying element on the output of the memory element,
- said common output amplifier having at least a first and a second input terminals,
- means for switching the pixel's signal on the common output line and the memory element's signal to respectively first and second amplifying elements of one column, and
- means for switching the two output signals of the amplifying elements of one column to respectively first and second input terminals of said common output amplifier.

Preferably, the switching means comprise at least one cross-bar switch.

According to another preferred embodiment, the image sensor further comprises before the amplifying element two parallel circuits being connected through switches to the common pixel output line, at least one circuit having said memory element. Preferably, both circuit have a memory element.

According to another preferred embodiment, said common pixel output line is being connected through switches to said memory element and said amplifying

element, where the offset of the amplifying element is stored on the memory element during a first phase of the read-out, and this offset is subtracted from the signal of the amplifying element during the second phase of the read-out.

The present invention is also related to a method of reading out an array of rows and columns of pixels in an image sensor as described hereabove according to the first embodiment, comprising the steps of:

- 10 - amplifying the output signals of essentially each pixel of one column in the first amplifying element thereby obtaining a set of amplified pixel output signals,
- amplifying the reference signals of essentially each pixel of one column in the second amplifying element,
- 15 thereby obtaining a set of amplified pixel reference signals,
- consecutively, for essentially each pixel of said column imposing the amplified pixel output signal to a first or a second terminal of said common output amplifier and
- 20 imposing the amplified pixel reference signal to a second or a first terminal of said common output amplifier, while switching the amplified pixel output signal to respectively said first and said second terminals for essentially each consecutive pixel of said
- 25 column, said reference signal being imposed to the other terminal of said common output amplifier.

A voltage can be imposed to a node. In this case, it means e.g. that the node is connected to a voltage source. The voltage source should be higher than the node,

30 i.e. it should have a lower impedance.

According to another preferred embodiment, the present invention is related to a method of reading out an array of rows and columns of pixels in an image sensor

as described hereabove in the second embodiment of the present invention, comprising the steps of :

- sampling the signal in a first phase and storing it in a memory element,
- 5 - sampling the signal in a second phase and possibly storing it in another memory element,
- subtracting said first signal from said second signal in a unique output circuit.

According to another preferred embodiment,
10 the present invention is related to a method of reading out an array of rows and columns of pixels in an image sensor as described in the third embodiment of the present invention, comprising the steps of :

- during a first phase, calibrating the output of the
15 amplifying element to a predetermined value,
- storing said value in a memory element during the application of a first signal of said pixel on the line,
- during a second phase, applying a second signal of said pixel on the line in order to have on the output a signal
20 proportional to the difference between first and second signals.

Another aspect of the present invention is related to a method of replacing an isolated pixel value in the image of an image sensor, being an array of pixels, and
25 wherein at least one current source is connected to the pixels, the method comprising the step of :

- limiting said isolated pixel value between or to an upper and/or a lower bound that is derived from the values of pixels in the immediate neighbourhood of the
30 said isolated pixel value.

Preferably, said upper and/or lower bounds are found by extrapolating the immediate neighbourhood pixel values towards a value that corresponds to the

position of said individual pixel in relation to the immediate neighbourhood pixels.

Said upper and/or lower bounds are found by extrapolating the values of a neighbour (V_1N) of the pixel
 5 having said isolated pixel value and of the neighbour thereafter (V_2N), the replacing pixel value being calculated as $V_1N + n \cdot (V_1N - V_2N)$, n being a real number.

The neighbourhood and the neighbourhood thereafter are on the same row of said array. Preferably,
 10 the upper bound is the maximum of a set of values, said set being determined as the pixel values (a, b, c, d, e) of pixels on the same row of said array as said isolated pixel, said upper bound being calculated as

$$c_{\max} = F(a, b, c, d), \text{ or } c_{\max} = G(E(a, b), E(e, d), E(b), E(d))$$

15 where F is a non-linear or linear function, G is a non-linear GE or linear function, E is an extrapolating function, wherein $c_{\max} = \text{MAX}(2b - a, 2d - e, b, d)$
 together with

$$c_{\min} = \text{MIN}(2b - a, 2d - e, b, d)$$

20 with $\text{MAX}()$ yielding the maximum, respectively the minimum of the arguments, the corrected c -value being obtained as

$$c = \text{MIN}(\text{MAX}(c, c_{\min}), c_{\max}).$$

25 Brief description of the drawings

Figure 1a represents a particular implementation of a column FPN cancellation method and the corresponding image sensor structure therefor.

30 Figure 1b represents an embodiment of a cross-bar switch used in the structure represented in Fig. 1a.

- Figure 2 describes another particular implementation of a column FPN cancellation method and the corresponding image sensor structure therefor.
- 5 Figure 3 describes a particular embodiment of an output block being used in the structure as represented in Fig. 2.
- Figure 4 represents the switching diagram for the read-out signal applied to the several
10 switches in the structure as represented in Fig. 2.
- Figures 5 represent another particular implementation of a column FPN cancellation method and the corresponding image sensor structure therefor, wherein Fig. 5a represents more
15 particularly one column in an array of pixels being connected to two different structures represented in details in Fig. 5b and 5c during a first phase and a second phase.
- 20 Figure 6 represents the specific topology used for the structure represented in Fig. 5b and 5c.
- Figure 7 represents the switching diagram for the read-out sequence to the several switches used in the structure represented in Fig. 6.
- 25 Figures 8a and 8b represent a method of correcting isolated white pixel values being present in an image composed by an array of pixels.

30 Brief description of preferred embodiments of the present invention

As a first object of the present invention, a first structure of an APS image sensor is represented in Fig. 1. References (X_{1j}) , (X_{2j}) and (X_{3j}) are three pixels

of a column of an image sensor. The pixel's signal on a common output line (l_j) is represented in particular by the column bus "K" in the present case and is fed to the optional buffer amplifier A_j , and/or stored on a memory element (capacitor C + switch S3), and fed to amplifier B_j . By the relative timing of the addressed pixel's reset pulse and the control of the switch S3, one can make that the pixel's signal and its reference level are available on amplifiers A_j , reps. B_j . The fact that the signal passes through the column amplifiers A_j and B_j , is a source of offset non-uniformity, which is column related and causes a vertical stripe-shaped FPN. More specifically, each column will feature an average "OV" offset voltage referred to the average of the other columns.

Switches (S1) and (S2) are crossbar switches. Suppose that they are in the forward direction either in crossed directions. Both switches S1 and S2 operate synchronously. In both cases, the signal on the capacitor C goes to the input of the output amplifier, and the signal on K goes to the + input of the output amplifier. Yet, the "OV" of the column will be positive in the one case and negative in the other case. Since the switches (S1)/(S2) are modulated, e.g. essentially turned direction at each new row ($i = 1, 2, 3$) of the image, the average offset of a column will be zero. For each individual pixel of a column, there will be indeed remain an offset which is + or - OV but this is a very small feature, and is not recognised by the eye as a stripe.

Another embodiment of the present invention is to suggest a read-out scheme for image sensors that suppresses the effects of non-uniformities caused by variations in pixels as well as variations in the output amplifiers. This read-out scheme can be used in sensors

that provide the output signal in terms of a difference. For example, in a sensor with integrating pixels, this difference is the voltage between the output when the pixel is on reset state and the output voltage after integration
5 time.

Namely the method suggests to subtract the signal when a pixel is reset from the signal after the integration time, in order to have a signal which is free from pixel variations. In order to avoid the introduction
10 of the non-uniform column amplifiers effects, the signal of the reset state as well as the signal after integration are sampled and held by the column read-out circuit. Finally, the subtraction is being carried out by a unique subcircuit at the sensor's output (D). This is detailed in Fig. 2.

15 For every row of pixels the read-out process is, of course, identical. Let us assume that the i^{th} row is selected. When pixels are reset, the switches controlled by the signal Φ_1 , are closed, thus the reset-level output of every pixel on the i^{th} row, namely x'_{ij} , is stored on the
20 corresponding memory element M_{rj} (which is in the present case a capacitor).

Then, the switches S_{4j} controlled by Φ_1 are opened and pixels start integrating the charge carriers produced by the impinging light. After the lapse of the
25 integration time, the switches S_{5j} controlled by Φ_2 are closed, thus storing the values of the pixel output to the memory element M_{sj} (also a capacitor). This value, for the pixel with coordinates ij is denoted as x^i_{ij} .

After the sample and hold phase for the two
30 voltages, x'_{ij} and x^i_{ij} , for the first column and by proceeding from the first column to the last, the

appropriate column read-out circuit is connected with the output.

When the i^{th} column has been selected, the signal $\Phi 3$ drives the switch $S6_j$ to lead the signal x_{ij}^r to the output modified according to the action of the column amplifier, so as a signal

$$y_{ij}^s = A_j x_{ij}^r + B_j \quad (1)$$

is led to block D (common output amplifier).

The block D is an easily realisable circuit with an output

$$z(n) = [y(n) - y(n-1)] \quad (2)$$

where $y(n)$ denotes the input as instant n .

A preferred embodiment of such output block (D) is described in details in Fig. 3. Therefore, the output signal will be free from variations in the characteristics of pixels and the column amplifiers.

$$y_{ij}^r - y_{ij}^s = A_j (x_{ij}^r - x_{ij}^s) \quad (3)$$

where A_j is easily reproducible, by example by using source followers as the local final phase of the column circuits (when $A_j = 2$, $B_j = -V_{thj}$).

Fig. 4 shows a switching diagram for the above-mentioned read-out circuit wherein $\Phi 3$ is controlling $S4_j$, $\Phi 4$ is controlling the switch $S5_j$ and $\Phi 5$ is controlling the switch $S6_j$.

According to another embodiment of the present invention, an attempt to overcome the problem of offset introduced by the column in a image sensor consisting of pixels is described in Figs. 5 & 6, which can be used with pixels that are read-out twice in every access. For example, in integrating pixels, one read

operation is being performed when the pixel is set on the reset phase (first phase) and the second read-out moment is after a certain integration time (second phase), the first phase is defined by a period wherein the read-out signal of the pixel is according a first state while the second phase is defined by a period such as an integration period where the read-out signal of the pixel is in another state.

In the first phase, when pixel output is V_1 , the capacitor C stores a charge :

$$10 \quad Q = C(V_{ac} - V_{out}) = C(V_{ac} - V_1 + V_{th}) \quad (4)$$

where V_{th} is the threshold voltage of μ .

During second phase, when pixel output is V_2 , the capacitor stores again charge Q which now can be expressed as :

$$15 \quad Q = C(V_{g\mu} - V_2) \quad (5)$$

where $V_{g\mu}$ is the gate voltage of μ .

From (4) and (5), we obtain :

$$V_{g\mu} = V_2 - V_1 + V_{ac} + V_{th} \quad (6)$$

Therefore :

$$20 \quad V_{out} = V_2 - V_1 + V_{ac} \quad (7)$$

i.e. the output voltage does not depend on the V_{th} (where variations in the V_{th} cause offsets in the signal V_{out}).

The column amplifier can be implemented by using the topology described in details in Fig. 6.

25 Switches S_7 , S_8 , S_9 , S_{10} and S_{11} are being controlled by signals Φ_5 and Φ_6 (when Φ_i is high, the corresponding switches are closed) as represented in Fig. 7.

According to a preferred embodiment
30 represented in Fig. 7, S_7 , S_8 and S_9 are controlled by Φ_5 while S_{10} and S_{11} are controlled by Φ_6 (when Φ_i is high, the corresponding switches are closed). This means that Φ_5

is describing the situation represented in Fig. 5b while $\Phi 6$ is representing the situation represented in Fig. 5c.

According to another aspect, the present invention is able to discriminate between isolated pixel faults and features in the real image. In the case of an image of a star covered sky, it should be noted that the fact that the image projected through a lens is never perfectly sharp. Even with good lenses, a star image is not projected on a single pixel. Always the point like source of the star will be smeared out over a central pixel and a few neighbours. In a 1-dimensional cross section, a star image will look like the image in Fig. 8a, while an isolated pixel fault will look like in Fig. 8b.

In the above simple example, the peak in Fig. 8b should be removed, while the peak in 8a should remain untouched.

The advantage is clear, only device faults are corrected while normal images are left untouched. The operation causes no visible image degradation in faultless parts of the image.

According to this second aspect of the present invention, a method to remove an isolated whiter or darker pixel from the image is suggested. This method consists in limiting the value of every individual pixel between an upper and/or a lower bound that is/are derived from the values of pixels in the intermediate neighbourhood of the said pixel.

Preferably, the upper and/or lower bounds are found by extrapolation of the neighbourhood pixel values towards the position of the said individual pixel. The upper and/or lower bound are/is a combination of one or several such 1-D or 2-D extrapolations done with different

methods, and/or from different sides of the said individual pixel.

Preferably, extrapolation is the linear extrapolation of a neighbour (N1) of the said individual pixel (IP) and the neighbour thereafter (N2). The extrapolated value is calculated as $2*N1-N2$ or more general: $N1 + n*(N1-N2)$ where the parameter n is a real number, typically between 0 and 3.

According to another preferred embodiment, the calculation of the upper bounds is performed by extrapolating values from the two sides of said individual pixels. The advantage is that only the pixels data in 1 line of an image are required, which saves memory and operations and allows straightforward implementation as a pipelined filter. Also such a filter is able to correct a vertical line defect.

In the example of Figs. 8a and 8b, five pixels in a neighbourhood (a 5-pixel "kernel") are taken. The experience is that smaller kernels do not yield good results. Larger kernels may give some improvements compared to the 5-pixel kernel.

CLAIMS

1. An image sensor comprising an array of rows (i) and columns (j) of pixels (X_{ij}), all the pixels of one column of the array being connected to at least one
5 common pixel output line (l_j) having at least one memory element (M_j) and at least a first amplifying element (A_j), all these amplifying elements (A_j) being connected to a common output amplifier (D), characterised in that the sensor further comprises:
- 10 - a second amplifying element (B_j) on the output of the memory element (M_j),
- said common output amplifier (D) having at least two input terminals,
- means (S1) for switching the pixel's signal on the common
15 output line (l_j) and the memory element's signal (M_j) to respectively third and second amplifying elements (A_j and B_j) of one column, and
- means (S2) for switching the two output signals of the
20 respectively first and second input terminals of said common output amplifier (D).
2. An image sensor as recited in claim 1, wherein said switching means comprise at least one cross-bar switch.
- 25 3. An image sensor comprising an array of columns and rows of pixels (X_{ij}), all the pixels of one column of the array being connected to at least one common pixel output line (l_j) having at least one memory element (M_j) and at least one amplifying element (A_j), all these
30 amplifying elements (A_j) being connected to a common output amplifier (D), characterised in that before the amplifying

element (A_j), the common pixel output line (l_j) is divided through switches ($S4_j$ and $S5_j$) in two parallel circuits, at least one circuit having said memory element (M_j).

4. An image sensor as recited in claim 3,
5 wherein both circuits have a memory element (M_{sj} and M_{rj}).

5. An image sensor comprising an array of columns and rows of pixels (X_{ij}), all the pixels of one column of the array being connected to at least one common pixel output line (l_j) having at least one memory element
10 (M_j) and at least one amplifying element (A_j), all these amplifying elements (A_j) being connected to a common output amplifier (D), characterised in that said common pixel output line (l_j) is being connected through switches ($S7_j$, $S8_j$, $S9_j$ and $S10_j$, $S11_j$) to a memory element (C_j) and an
15 amplifying element (μ_j), where the offset of the amplifying element is stored on the memory element during a first phase of the read-out, and this offset is subtracted from the signal of the amplifying element during the second phase of the read-out.

20 6. A method of reading out an array of rows and columns of pixels (X_{ij}) of an image sensor according to claim 1, comprising the steps of :

- amplifying the output signals of essentially each pixel of one column in the first amplifying element (A_j)
25 thereby obtaining a set of amplified pixel output signals,
- amplifying the reference signals of essentially each pixel of one column in the second amplifying element (B_j), thereby obtaining a set of amplified pixel
30 reference signals,
- consecutively, for essentially each pixel ($i = 1, 2, 3$)

of said column imposing the amplified pixel output signal to a first or a second terminal of said common output amplifier (D) and imposing the amplified pixel reference signal to a second or a first terminal of said common output amplifier (D), while switching the amplified pixel output signal to respectively said first and said second terminals for essentially each consecutive pixel of said column, said reference signal being imposed to the other terminal of said common output amplifier.

7. A method of reading out an array of rows and columns of pixels (X_{ij}) of an image sensor as recited in claim 3, comprising the steps of :

- sampling the signal in a first phase and storing it in a memory element (M_{ij}),
- sampling the signal in a second phase and possibly storing it in another memory element,
- subtracting said first signal from said second signal in a unique output circuit (D).

8. Method as recited in claim 7, wherein said first phase is the reset phase and said second phase is after the integration period.

9. A method of reading out an array of rows and columns of pixels (X_{ij}) of an image sensor as recited in claim 5, comprising the steps of :

- during a first phase, calibrating the output of the amplifying element to a predetermined value,
- storing said value in a memory element during the application of a first signal of said pixel on the line,
- during a second phase, applying a second signal of said pixel on the line in order to have on the output a signal proportional to the difference between first and second signals.

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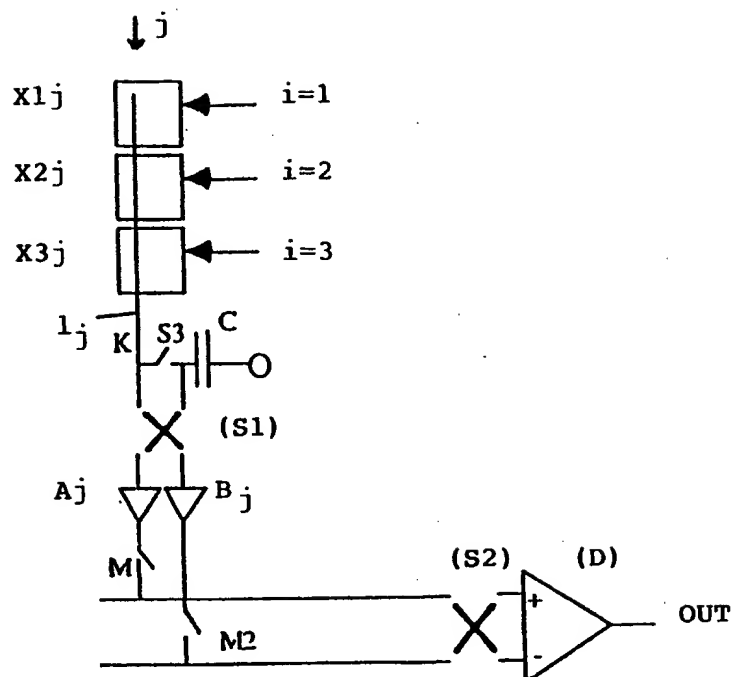


FIG. 1a

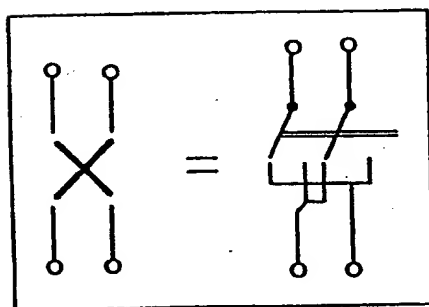


FIG. 1b

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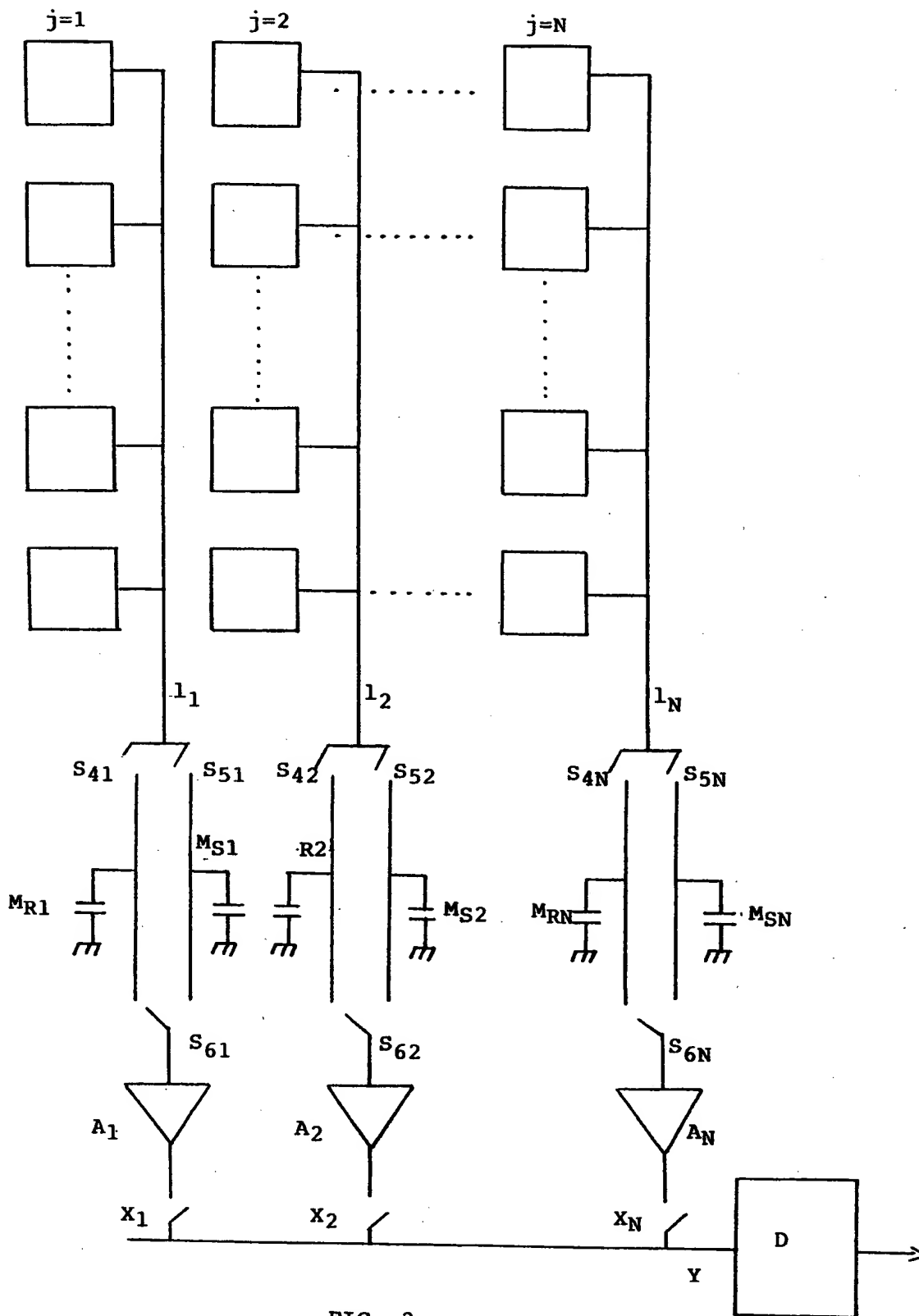
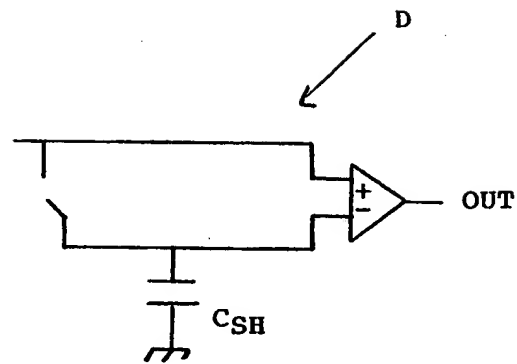
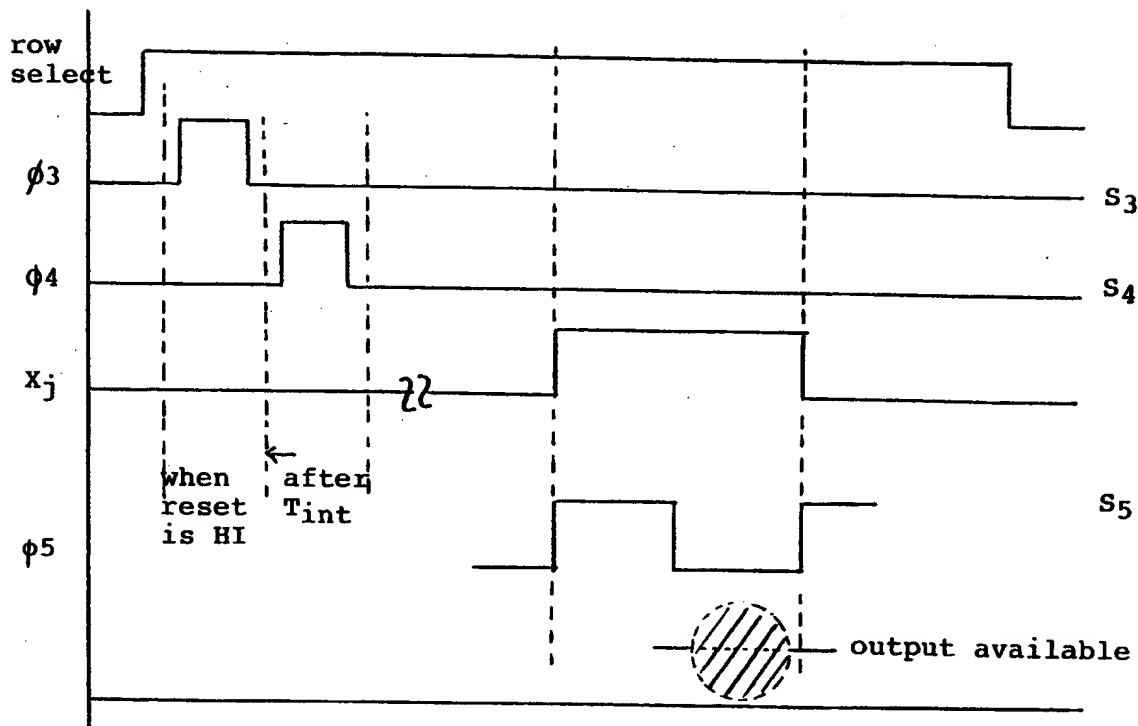
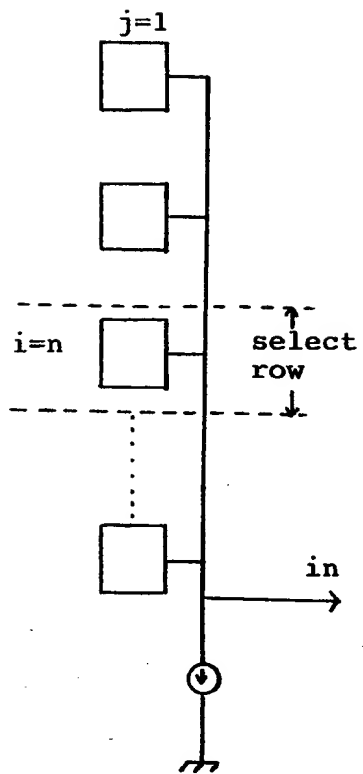
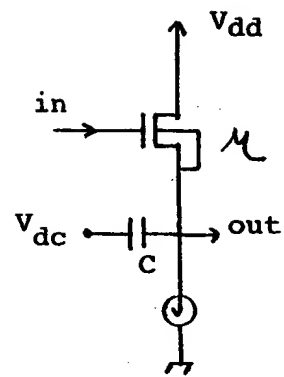
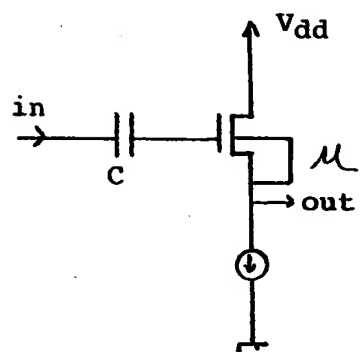


FIG. 2

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FIG. 3FIG. 4

FIG. 5aFIG. 5bFIG. 5c

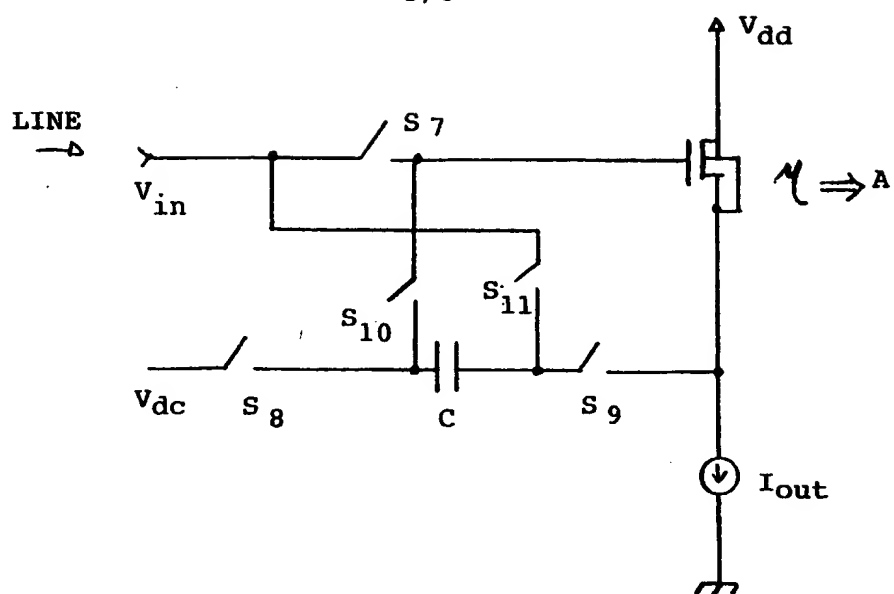


FIG. 6

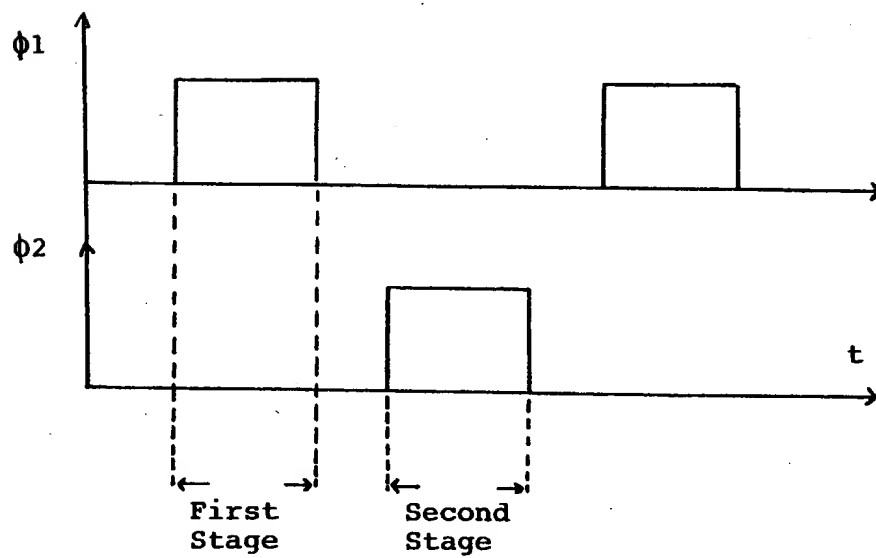


FIG. 7

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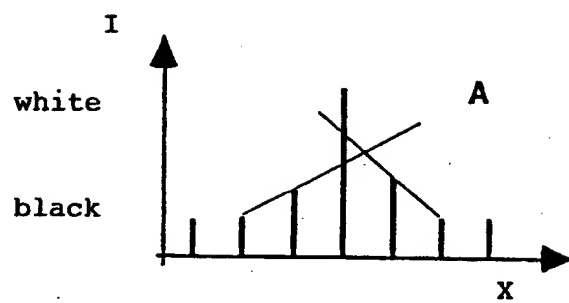


FIG. 8a

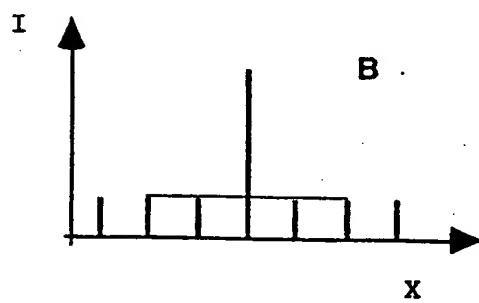


FIG. 8b

INTERNATIONAL SEARCH REPORT

Internat'l Application No

PCT/BE 98/00139

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04N3/15 H04N5/217

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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X	MARTIN W J ET AL: "DYNAMIC OFFSET NULL" IBM TECHNICAL DISCLOSURE BULLETIN, vol. 23, no. 9, February 1981, page 4195/4196 XP002052268 see the whole document ---	5,9
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☒ Further documents are listed in the continuation of box C.

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Date of the actual completion of the international search

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INTERNATIONAL SEARCH REPORT

International Application No

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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INTERNATIONAL SEARCH REPORT

Information on patent family members

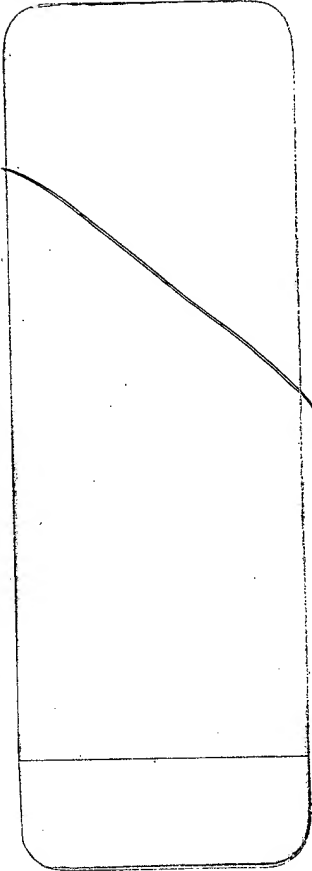
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